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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/763,304
Filing Date: January 23, 2004
Appellant(s): MATHEW ET AL.

Stephen B. Ackerman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01/22/2008 appealing from the Office action mailed April 03, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

In page 11 of the Appeal Brief, the rejection of claim 23 should be read:

The rejection of Claim 23 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092) taken with Deshpande et al (US 6,512,266) and Wieczorek et al (US 6,274,511), and further in view of Wu (US 6,130,135).

And the rejection of claims 5 and 10 should be read:

The rejection of Claims 5 and 10 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen (US 6,084,279), and further in view of Deshpande et al (US 6,512,266).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,818,092	Bai et al.	10-1998
6,512,266	Deshpande et al.	1-2003
6,130,135	Wu	10-2000
6,274,511	Wieczorek et al.	8-2001
5,625,217	Chau et al.	4-1997
6,084,279	Nguyen et al.	7-2000
US 2002/0192932 A1,	Tsai et al.,	Dec. 19, 2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-6, 9-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 5,818,092; hereinafter Bai) in view of Deshpande et al. (US 6,512,266; hereinafter Deshpande).

With reference to Figs. 2A-2C, Bai teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer **202** on said semiconductor substrate (Fig. 2A);

forming a conductive layer **206** (metal layer of TiN or TaN) on said gate insulator layer (col. 4, lines 18-19), wherein said conductive layer is formed of a single material *(note that the TiN or TaN is considered as a single material for the reason set forth in the previous Office action dated 9/6/06. That is, the claimed limitation "single material" does not necessarily mean a single metallic element, hence the TiN or TaN is considered as a single material consisting of two elements. An analogy is water in that water is a single material consisting of hydrogen and oxygen)*;

forming an amorphous silicon (a-Si) layer **208** (about 500 Å), wherein said amorphous silicon layer is formed of a single material, **directly** on said conductive layer **206** (col. 4, lines 33-55); ***(note that the a-Si layer 208 is formed immediately after formation of the underlying conductive layer 206, thus precluding the formation of any intervening material. Accordingly, newly added limitation "without inclusion of any interceding steps immediately..." is anticipated by the reference)***

defining a conductive gate structure and an overlying a-Si shape, on said gate insulator layer **202** (Fig. 2B and col.4, lines 58-64);

removing portion of said gate insulator **202** layer not covered by said conductive gate structure (Fig. 2B);

forming a first doped region **214** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. 2B and col. 5, lines 1-5);

forming nitride spacers **212** on the sides of said conductive gate structure and on the sides of said a-Si shape **208** (Fig. 2B and col. 5, lines 6-11);

forming a second doped region **216** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said nitride spacers **212** (Fig. 2B and col. 5, lines 11-15);

forming a metal layer **218,** wherein said metal layer is formed of a single material such as Ti, Co, Pd, Pt, or Ni by sputtering (physical vapor deposition) (Fig. 2B and col. 5, lines 33-60) ;

performing a rapid thermal annealing (RTA) procedure to form first metal silicide regions **220** from an overlying first portion of said metal layer and from a top portion of said second doped region **216,** and to form a second metal silicide region **220** directly on said conductive gate structure from an overlying second portion of said metal layer via total consumption of said a-Si shape **208,** while third portions of said metal layer located on said nitride spacers **212** remain unreacted (col. 6, lines 1-10); and

removing unreacted portions of said metal layer located on said nitride spacers **212** (Fig. 2C and col. 6, lines 50-58).

Also, see col. 4, lines 38-39 for the teaching that the a-Si layer **208** is completely consumed during the silicide reaction.

Bai differs from the claims in not disclosing that the nitride spacers **212** are formed of a composite material comprises an oxide liner and a nitride layer. Deshpande teaches a composite insulator spacer comprises an oxide liner **22** and a nitride layer **24**, wherein the oxide liner **22** having a thickness of 2 - 400 Å (col. 5, lines 62-65) and the nitride layer **24** having a thickness of 20 - 1,000 Å (col. 6, lines 9-32). It would have been obvious to one for ordinary skill in the art to form the nitride spacer **212** consisting of an oxide liner and a nitride layer having thicknesses as suggested by Deshpande because the oxide liner acts as a buffer to reduce stress generated by the overlying nitride layer and therefore improves insulation between the gate electrode and source/drain regions.

For claims 2-4, see col. 5, lines 25-26 in Bai.

As for claims 5 and 6, Bai differs from the claims in not disclosing that a high dielectric constant (high-k) material is used for the gate insulator layer **202.** Deshpande teaches a gate insulator layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). The subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Bai's teaching by forming the gate insulator layer **202** using the high-k dielectrics because the selection of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art.

For claim 9, see col. 4, line 62-64 in Bai.

For claim 10, see the thicknesses of the oxide liner 22 and the nitride layer 24 mentioned above.

For claim 11, see Bai col. 5, lines 42-60 for the thickness of the metal layer 218.

For claim 12, see Bai col. 6, lines 5-15.

B. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Despande as applied to claims 1-6, 9-12 and 14 above, and further in view of Wu (US 6,130,135).

The combined process of Bai and Deshpande teaches a method as described above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

C. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Deshpande as applied to claims 1-6, 9-12 and 14 above, and further in view of Tsai et al. (US 2002/0192932; hereinafter Tsai) and Wieczorek et al. (US 6,274,511; hereinafter Wieczorek).

The combined process of Bai and Deshpande teaches a method as noted above. The combination differs from the claim in not disclosing that the unreacted refractory metal portions **218** are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH – H_2SO_4 as claimed. Wieczorek teaches that unreacted refractory metal is removed using typical solution such as $HCl:H_2O_2$ and $H_2SO_4:H_2O_2$ (col. 6, lines 37-43; hereinafter solution A). Tsai teaches unreacted refractory metal is removed using a solution such as $NH_4OH:H_2O_2$ (para. [0026]; hereinafter solution B). Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal **218** in the combined process of Bai and Deshpande using a mixture comprises $HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

D. Claims 16-21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Deshpande as applied to claims 1-6, 9-12 and 14 above, and further in view of Wieczorek cited above.

The combined process of Bai and Deshpande teaches a method as noted above, including the first RTA step to form the silicide layers **220**. Note that since claim 16 employs "comprising" format, the claimed limitation " a metal gate structure and an overlying amorphous silicon shape" recited in claim 16 does not necessarily limit to a

gate structure consisting of a metal layer and an overlying amorphous silicon layer, hence Bai's gate structure consists of a composite **metal layer 206/polysi 204** and an overlying amorphous silicon shape **208** reads on the aforementioned limitation.

The combination differs from the claims in the step of performing a second anneal procedure.

Wieczorek teaches that after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Bai and Deshpande by performing a second annealing step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claims 25 and 26, see Deshpande, col. 5, line 51 and col. 6, line 17 for the teaching that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art. It is noted that applicants did not challenge the Examiner's Official notice in response to the previous Office action.

E. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Despande and Wieczorek as applied to claims 16-21 and 24-28 above, and further in view of Wu cited above.

The combined process of Bai taken with Deshpande and Wieczorek teaches a method as noted above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

F. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Deshpande and Wieczorek as applied to claims 16-21 and 24-28 above, and further in view of Tsai cited above.

The combined process of Bai taken with Deshpande and Wieczorek teaches a method as noted above, including the teaching of using the aforementioned solution A to remove unreacted refractory metal **218**. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH - H_2SO_4. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above.

Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal **218** in the combined process using a mixture comprises $HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested

by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

G. Claims 1-4, 6-7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (US 5,625,217; hereinafter Chau) in view of Nguyen et al. (US 6,084,279; hereinafter Nguyen).

With reference to Figs 4A-4G, Chau teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer **502** (20-200 Å) on said semiconductor substrate (col. 4, line 9);

forming a conductive layer **504** of *a single material* including sputtered TiN, W, and Co having thickness 20-2,000 Å on said gate insulator layer (col. 2, line 13; col. 4, lines 14-45);

forming a polysilicon layer **506** (3,500 Å) directly on said conductive layer (col. 4, lines 53-60);

(note that the polysilicon layer 506 is formed immediately after formation of the underlying conductive layer 504, thus precluding the formation of any intervening material. Accordingly, newly added limitation "without inclusion of

any interceding steps immediately..." is met by the reference except that layer 506 is of polysilicon instead of amorphous silicon as claimed)

defining a conductive gate structure **513** and an overlying polysilicon shape **512**, on said gate insulator layer **502** (Fig. 4B);

removing portion of said gate insulator layer **502** not covered by said conductive gate structure **513** (col. 6, lines 16-17);

forming a first doped region **514a/514b** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. 4C and col. 5, lines 27-30);

forming composite insulator spacers **518a/518b** on the sides of said conductive gate structure and on the sides of said semiconductor shape (Fig. 4E and col. 5, lines 43-53);

forming a second doped region **520a/520b** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers **518a/518b** (Fig. 4E and col. 6, lines 1-3);

forming a metal layer **522** of *a single material* including Ti and W (Fig. 4F and col. 6, lines 22-24) ;

performing an anneal procedure to form first metal silicide regions **524** from an overlying first portion of said metal layer **522** and from a top portion of said second doped region **520a/520b ,** and to form a second metal silicide region on said conductive gate structure from an overlying second portion of said metal layer **522** and

from a portion of said polysilicon shape **512,** while third portions of said metal layer located on said composite insulator spacers **518a/518b** remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers **518a/518b** (Fig. 4G and col. 6, lines18-35).

Chau differs from the claims in not disclosing that a) the semiconductor layer **506** is of amorphous silicon and b) the metal silicide **524** is formed via total consumption of said amorphous silicon shape.

For issue a), Nguyen teaches a metal gate structure in which amorphous silicon **68** or polysilicon can be used for the gate structure. The amorphous silicon is doped either insitu (i.e., during deposition) or during separate doping step (col. 5, lines 25-27).

It would have been obvious to one of ordinary skill in the art to modify Chau's teaching by replacing the polysilicon layer **506** with amorphous silicon because the substitution of art recognized equivalents as shown by Nguyen would have been within the level of one skilled in the art, and the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination (MPEP 2144.07).

For issue b), Nguyen teaches a method for making a metal gate structure in which silicide **85** is formed via total consumption of amorphous silicon gate structure **68** (Figs. 7-8 and col. 5, lines 65-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau's teaching by forming silicide **524** via total consumption of the amorphous silicon gate **512** (modified polysilicon mentioned above)

as suggested by Nguyen because converting totally the gate electrode **512** to metal silicide would reduce the gate resistance and hence improve the performance of the device.

For the limitation of claim 4, see col. 4, lines 20-22 and col. 6, lines 50-57.

H. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen as applied to claims 1-4, 6-7, and 9 above, and further in view of Deshpande cited above.

The combined process Chau and Nguyen teaches a process for forming a MOSFET device as noted above. The combination differs from the claims in not disclosing a) a high dielectric constant (high-k) material is used for the gate dielectric layer **502** and b) the thickness of the composite insulator spacer **518a/518b**.

Deshpande teaches a gate dielectric layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). Furthermore, Deshpande teaches the thickness of an insulator spacer of a MOSFET device having LDD regions is typically from about 20 Å to about 1,000 Å (col. 6, lines 9-32).

As for issue a), the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined process by forming the gate dielectric layer **502** using the high-k dielectrics because the substitution of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art, and the selection of a known material

based on its suitability for its intended use supported a prima facie obviousness determination (MPEP 2144.07).

As for issue b), it would have been obvious to one for ordinary skill in the art to form the composite insulator spacer in Chau having a thickness suggested by Deshpande because such thickness for an insulator spacer is typical in the art, and utilizing a known value to made the same would have been within the level of one skilled in the art.

I. Claims 16-22, 24-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen and Deshpande as applied to claims 5 and 10 above, and further in view of Wieczorek cited above.

The combination of Chau, Nguyen and Deshpande teaches a method as described above. The combined process differs from the claims in that the combined process performs the annealing once instead of twice as claimed.

Wieczorek teaches after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Chau, Nguyen and Deshpande by performing a first anneal step using RTA to form metal silicide and then performing a second RTA step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claims 25 and 26, see Deshpande, col. 5, line 51 and col. 6, line 17 for the teaching that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art. It is noted that applicants did not challenge the Examiner's Official notice in response to the previous Office action.

For claim 28, see Wieczorek, col. 6, lines 10-15 for the parameters of the first RTA.

K. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen, Deshpande and Wieczorek as applied to claims 16-22, 24-26 and 28 above, and further in view of Wu cited above.

The combination teaches a process as described above. The combined process differs from the claim in not disclosing that the a-Si layer is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

L. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen, Deshpande and Wieczorek as applied to claims 16-22, 24-26 and 28 above, and further in view of Tsai cited above.

The combination teaches a method as described above, including the teaching of using the aforementioned solution A (see Wieczorek) to remove unreacted refractory metal. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH - H_2SO_4. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above. Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process using a mixture comprises $HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

(10) Response to Argument

a) Regarding the rejection of claims 1-6, 9-12, and 14 under 35 U.S.C 103(a) as being unpatentable over Bai et al. in view of Deshpande, appellants argue: "*A key feature of applicant's process invention is the formation of a metal silicide region, such as region 10c in Fig. 7, via total consumption of amorphous shape 4b, Fig 6. This will result in the desirable situation in which metal silicide region 10c resides directly on*

underlying conductive shape 3b, without any other layers between. This will, in contrast to having interceding materials between, allow the lowest gate structure resistance.", and "*...Bai et al. use a layer between the metal and conductive layers to avoid the silicide process from unwanted attack of the underlying conductive gate structure. It is clear that Bai et al do use this protective layer, layer 206 in Fig. 2a- 2c, and this layer unlike applicant's invention remains as a component of their final composite conductive gate structure. Applicant clearly in independent Claim 1 states no interceding steps between deposition of the conductive layer and the amorphous silicon thus precluding the use of a costly and complex stop layer deposition. In addition applicant's Claim 1 states the metal silicide region is formed directly on underlying conductive gate structure. This is surely significant process differences when compared to the Bai et al prior art.*" (page 13 of the Brief).

In response, the Examiner respectfully disagrees with appellants' arguments for the following reasons:

- The issue here is whether or not the Examiner has correctly interpreted the teachings of prior art to read on process steps as claimed, not the use of a protective layer in the silicidation process because neither independent claim 1 nor independent claim 16 recites such protective layer.

- Turning to Bai's reference, Fig. 2A shows a gate insulator layer **202** formed on a semiconductor substrate, a polysi (or amorphous silicon) layer **204** formed on the gate insulator layer **202,** a TiN or TaN metal layer **206** (i.e., inherently conductive)

formed on the gate insulator layer **202,** and an amorphous silicon (a-Si) layer **208** formed directly on the metal layer **206.** As mentioned in the rejection, it is the metal layer **206**, not polysi layer **204,** that the Examiner relied in the rejection to show anticipation of the claimed conductive layer (emphasis added). Accordingly, the formation of the a-Si layer **208** is immediately and directly on the conductive layer **206** without inclusion of any interceding steps as claimed. Furthermore, as noted in the Advisory Action dated 07/17/2007, claim 1 employs "comprising" format which does not exclude the inclusion of polysi layer **204,** hence Bai's conductive layer **206,** which is a portion of the composite gate structure comprises metal layer **206/**polysi **204,** reads on the claimed conductive gate structure. Accordingly, metal silicide region **220** (Fig. 2C) is formed directly on the conductive gate structure **204/206** via total consumption of the a-Si layer **208** (col. 4, lines 38-39 in Bai) without the use of a stop layer residing on the top surface of the conductive gate structure **204/206**.

- Appellants do not argue the appropriation of applying the secondary reference to Deshpande by the Examiner to show the formation of the claimed composite insulator spacers would have been obvious to one skilled in the art.

b) Regarding the rejection of Claim 8 under 35 U.S.C. 103(a) as being unpatemable over Bai (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and further in view of Wu (US 6,130,135), appellants argue: *" the combination of the above prior art does not present applicant's invention where a metal silicide region is formed directly on an underlying conductive gate structure without the use of a stop layer used on the top surface of the underlying conductive gate shape."*

In response, the Examiner respectfully disagrees. As mentioned in the above paragraph, the "comprising" format employed in claim 1 permits broad interpretation of the claim in that the composite conductive gate structure **204/206** of the prior art reads on the claimed conductive gate structure. As a result, the metal silicide region **220** (Fig. 2C) is formed directly on an underlying conductive gate structure **204/206** without the use of a stop layer used on the top surface of the underlying conductive gate shape. Appellants do not argue the appropriation of applying the secondary reference to Wu by the Examiner to show the formation of the claimed a-Si layer by means of LPCVD or PECVD would have been obvious to one skilled in the art.

c) Regarding the rejection of Claim 15 under USC 103(a) as being unpatentable over Bai (US 5,818,092) taken with Deshpande (US 6,512,266 B1), and further in view of Tsai (US 2002/0192932) and Wieczorek (US 6,274,511).

The Examiner's responses addressed in the above paragraph a) and b) are repeated herein. Appellants do not argue the appropriation of applying secondary references to Tsai and Wieczorek by the Examiner to show wet etching of unreacted refractory metal portions **218** using a solution comprises of HCl -H_2O_2 -NH_4OH- H_2SO_4 would have been obvious to one skilled in the art.

d) Regarding the rejection of Claims 16- 21, and 24- 28 under USC 103(a) as being unpatentable over Bai (US 5,818,092) taken with Desphpande (US 6, 512,266 B1), and further in view of Wieczorek (US 6,274,511).

The Examiner's responses addressed in the above paragraph a) and b) are repeated herein. Appellants do not argue the appropriation of applying secondary reference to Wieczorek by the Examiner to show the claimed step of performing a second anneal procedure recited in claim 16 would have been obvious to one skilled in the art.

e) Regarding the rejection of claim 23 under USC 103(a) as being unpatentable over Bai (US 5,818,092) taken with Deshpande (US 6,512,266 B 1) and Wieczorek (US 6,274,511), and further in view of Wu (US 6,130,135).

The Examiner's responses addressed in the above paragraph a) and b) are repeated herein. Appellants do not argue the appropriation of applying secondary reference to Wu by the Examiner to show the formation of the claimed a-Si layer by means of LPCVD or PECVD would have been obvious to one skilled in the art.

f) Regarding the rejection of Claim 31 as being unpatentable over Bai (US 5,818,092), taken with Deshpande (US 6,512,266) and Wieczorek (US 6,274,511), and further in view of Tsai (US 2002/0192932).

The Examiner's responses addressed in the above paragraph a) and b) are repeated herein. Appellants do not argue the appropriation of applying secondary references to Wieczorek and Tsai by the Examiner to show wet etching of unreacted refractory metal portions **218** using a solution comprises of HCl -H_2O_2 -NH_4OH- H_2SO_4 would have been obvious to one skilled in the art.

g) Regarding the rejection of Claims 1- 4, 6-7, and 9, under USC 103(a) as being unpatentable over Chau (US 5,625,217) in view Nguyen (US 6,084,279), appellants argue : "*As clearly described in independent Claim 1 of applicant's process invention the desired metal silicide region is formed, directly on the underlying conductive gate structure via total consumption of the amorphous silicon shape. The Chau et al prior, as shown in Fig. 4g, clearly show metal silicide layer 524 formed via only via partial consumption of silicon layer 512. The Nguyen et al prior art only describe fabrication of a gate structure never claiming metal silicide formation on an underlying gate structure achieved via total consumption of the components, a metal layer an amorphous silicon layer. Therefore there is no evidence that the combination of the Chau and Nguyen art could lead one to applicant's process.*"

In rebuttal, the Examiner respectfully disagrees. Chau's reference was employed in the rejection to show all features of the claims except for the semiconductor layer **506** (Fig. 4A) is of amorphous silicon and the metal silicide **524** (Fig. 4G) is formed via total consumption of said amorphous silicon shape. It is the Nguyen reference that cures the deficiency in Chau. That is, Nguyen provides logical reasons as to why one of ordinary skill in the art would be motivated to make the combination as addressed in the rejection. Appellants are reminded that it is axiomatic that one cannot show nonobviousness by attacking references individually where the rejection, as here, is based on a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For example, appellants argue that Chau does not teach or suggest the claimed features as

mentioned above. However, the combined process of Chau and Nguyen, not Chau nor Nguyen alone, is employed in the rejection to show an amorphous silicon layer is formed directly on the conductive layer **504** of a single material such as TiN, W, or Co, and said amorphous silicon layer is totally consumed by the subsequent silicidation process. That is, Chau's reference is relied in the rejection to show the **immediate** formation of the polysilicon layer **506** directly on the conductive layer **504** and therefore **without any interceding steps**, which in turn directly overlays gate insulator **502**. On the other hand, Nguyen' s reference, not Chau, is relied in the rejection to provide logical reason as to why one skilled in the art would be motivated to replace the polysilicon layer **506** with an art-recognized equivalent material such as amorphous silicon (col. 5, lines 25-27), and thereafter total consumption of said amorphous layer in the silicidation process (Figs 7-8 and col. 5, lines 65-66). Thus, the claims are met by the combined teachings of the references, not by a single reference as alleged by appellants.

h) Regarding the rejection of Claims 5 and 10 under USC 103(a) as being unpatentable over Chau (US 5,625,217) taken with Nguyen (US 6,084,279), and further in view of Deshpande (US 6,512,266 B1).

The Examiner's response addressed in the above paragraph g) is repeated herein. Appellants do not argue the appropriation of applying the secondary reference to Deshpande by the Examiner to show the use of a high-k dielectric material for the gate insulator layer and the thickness of the composite insulator spacers would have been obvious to one skilled in the art.

i) Regarding Rejection of Claims 16 - 22, 24 - 26 and 28 under USC 103(a) as being unpatentable over Chau (US 5,625,217) taken with Nguyen (US 6,084,279) and Desphande (US 6,512,266), and in further view of Wieczorek (US 6,274,511).

The Examiner's response addressed in the above paragraph g) is repeated herein. Appellants do not argue the appropriation of applying the secondary reference to Wieczorek by the Examiner to show the claimed step of performing a second anneal procedure recited in claim 16 would have been obvious to one skilled in the art.

j) Regarding Rejection of Claim 23, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen (US 6,084,279), Desphande (US 6,512,266) and Wieczorek (US 6,274,511), and in further view of Wu (US 6,130,135).

The Examiner's response addressed in the above paragraph g) is repeated herein. Furthermore, the combined process of Chau and Nguyen result in a method in which metal silicide region **524** is formed by total consumption of the amorphous silicon gate **512** (polysi is replaced with amorphous silicon as suggested by Nguyen). Thus, the metal silicide region **524** is formed directly on an underlying conductive gate structure **510** without the use of a stop layer used on the top surface of the underlying conductive gate shape **510.** Appellants do not argue the appropriation of applying the secondary reference to Wu by the Examiner to show the formation of the claimed a-Si layer by means of LPCVD or PECVD would have been obvious to one skilled in the art.

k) Regarding the the rejection of Claim 31 under USC 103(a) as being unpatentable over Chau (US 5,625,217) taken with Nguyen (US 6,084,279), Desphande (6,512,266) and Wieczorek (US 6,274,511), and in further view of Tsai (US 2002/0192932).

The Examiner's response addressed in the above paragraph g) is repeated herein. Appellants do not argue the appropriation of applying secondary references to Wieczorek and Tsai by the Examiner to show wet etching of unreacted refractory metal portions using a solution comprises of HCl -H_2O_2 -NH_4OH- H_2SO_4 would have been obvious to one skilled in the art.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Trung Dang/

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